AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Currently Amended) A scanning conversion apparatus, comprising:

a first converter converting input interlaced scan data into progressive scan data; and

a second converter converting the progressive scan data output from the first converter to interlaced scan data, the second converter including,

a memory configured to store progressive scan data and further configured to generate a write signal, and

an address controller selectively applying write and read addresses to the memory based on the write signal output from the memory, the write and read addresses being for storing progressive scan data in the memory.

2. (Withdrawn) The apparatus of claim 1, wherein the first converter converts the input interlaced scan data into progressive scan data according to a technique selected from different techniques.

3. (Withdrawn) The apparatus of claim 2, wherein the different techniques include,

a spatial interpolation technique the involves performing spatial interpolation on a current field of the input interlaced scan data to produce a field of complementary scan data that together with the current field represents a frame of the progressive scan data;

an alternative field output technique in which two consecutive fields of the input interlaced scan data are alternately output on a scan line by scan line basis to produce a frame of the progressive scan data;

and a spatial/temporal interpolation technique that involves performing directionally adaptive spatial interpolation adaptively combined with temporal interpolation using the current field, at least one previous field and at least one subsequent field of the input interlaced scan data to produce a field of complementary scan data that together with the current field represents a frame of progressive scan data.

4. (Original) The apparatus of claim 1, wherein the second converter converts the progressive scan data output from the first converter to interlaced scan data such that the interlaced scan data output by the second converter is synchronized with the progressive scan data output from the first converter.

5. (Currently Amended) The apparatus of claim 1, wherein the second converter further comprises:

a counter generating the counter signal in the form of count values at a progressive scanning frequency such that the count values are associated with a period of the progressive scan data;

~~a memory;~~

a write address generator generating write addresses for writing progressive scan data into the memory based on output of the counter; and

a read address generator generating read addresses for outputting the progressive scan data written into the memory as interlaced scan data based on output of the counter.

6. (Canceled).

7. (Currently Amended) The apparatus of claim [[6]] 1, wherein the address controller controls the application of the write and read addresses to the memory such that a scan line of interlaced scan data is read from the memory while progressive scan data for the scan line is written to the memory.

8. (Withdrawn) The apparatus of claim 5, wherein the counter generates count values associated with different periods of the progressive scan data based on whether the progressive scan data is being converted into one of an odd and an even field of interlaced scan data.

9. (Withdrawn) The apparatus of claim 8, wherein the counter generates count

values associated with a odd scan line and a subsequent even scan line of progressive data when the progressive scan data is being converted into an odd field of interlaced scan data, and the counter generates count values associated with an even scan line and a subsequent odd scan line of progressive scan data when the progressive scan data is being converted into an even field of interlaced scan data.

10. (Original) The apparatus of claim 5, wherein the counter generates count values associated with two consecutive scan lines of progressive scan data.

11. (Original) The apparatus of claim 10, wherein the write address generator, comprises:

a first write address generator generating first write addresses associated with a first of the two consecutive scan lines based on the count values;

a second write address generator generating second write addresses associated with a second of the two consecutive scan lines based on the count values; and

a write address controller selectively outputting one of the first and second write addresses based on whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data.

12. (Original) The apparatus of claim 11, wherein the write address controller

receives a control signal indicating whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data.

13. (Original) The apparatus of claim 10, wherein the read address generator converts the count values into read addresses associated with one scan line of interlaced scan data.

14. (Currently Amended) The apparatus of claim 1, wherein the second converter, further comprises:

~~a memory;~~

a timer configured to generate the counter signal indicating a timing of two consecutive scan lines of the progressive scan data;

a write address generator receiving a control signal indicating which of the two consecutive scanning lines to write into the memory, and the write address generator generating write addresses for the indicated scanning line based on the timing indicated by the timer; and

a read address generator generating read addresses to read the written line from the memory, the read address generator beginning the generation of the read addresses based on the timing indicated by the timer.

15. (Currently Amended) A scanning conversion apparatus, comprising:

an interlaced-to-progressive converter and a progressive-to-interlaced converter connected in series to generate interlaced scan data synchronized

with progressive scan data output by the interlaced-to-progressive converter, the progressive-to-interlaced converter including,

a memory configured to store progressive scan data and further configured to generate a write signal,

an address controller selectively applying the write and read addresses to the memory based on the write signal output from the memory, the write and read addresses being for storing the progressive scan data.

16. (Currently Amended) A progressive-to-interlaced scan data converter, comprising:

a counter generating count values at a progressive scanning frequency such that the count values are associated with a period of progressive scan data;

a memory configured to generate a write signal;

a write address generator generating write addresses for writing progressive scan data into the memory based on output of the counter; and

a read address generator generating read addresses for outputting the progressive scan data written into the memory as interlaced scan data; and

an address controller selectively applying the write and read addresses to the memory based on the write signal generated by the memory.

17. (Canceled).

18. (Currently Amended) The converter of claim [[17]] 16, wherein the address controller controls the application of the write and read addresses to the memory such that a scan line of interlaced scan data is read from the memory while progressive scan data for the scan line is written to the memory.

19. (Withdrawn) The converter of claim 16, wherein the counter generates count values associated with different periods of the progressive scan data based on whether the progressive scan data is being converted into one of an odd and an even field of interlaced scan data.

20. (Withdrawn) The converter of claim 19, wherein the counter generates count values associated with a odd scan line and a subsequent even scan line of progressive data when the progressive scan data is being converted into an odd field of interlaced scan data, and the counter generates count values associated with an even scan line and a subsequent odd scan line of progressive scan data when the progressive scan data is being converted into an even field of interlaced scan data.

21. (Original) The converter of claim 16, wherein the counter generates count values associated with two consecutive scan lines of progressive scan data.

22. (Original) The converter of claim 21, wherein the write address generator, comprises:

a first write address generator generating first write addresses associated with a first of the two consecutive scan lines based on the count values;

a second write address generator generating second write addresses associated with a second of the two consecutive scan lines based on the count values; and

a write address controller selectively outputting one of the first and second write addresses based on whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data.

23. (Original) The converter of claim 22, wherein the write address controller receives a control signal indicating whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data.

24. (Original) The converter of claim 21, wherein the read address generator converts the count values into read addresses associated with one scan line of interlaced scan data.

25. (Currently Amended) A progressive-to-interlaced scan data converter, comprising:

a memory configured to generate a write signal;

a timer indicating a timing of two consecutive scan line of progressive scan data;

a write address generator receiving a control signal indicating which of the two consecutive scanning lines to write into the memory, and the write address generator generating write address for the indicated scanning line based on the timing indicated by the timer; and

a read address generator generating read addresses to read the written line from the memory, the read address generator beginning the generation of the read addresses based on the timing indicated by the timer; and

an address controller selectively applying the write and read addresses to the memory based on the write signal.

26. (Currently Amended) A method of scanning conversion, comprising:

converting input interlaced scan data into progressive scan data; and

converting the progressive scan data into output interlaced scan data, the converting the progressive scan data into output interlaced scan data including,

writing and reading progressive scan data to and from a memory based on write and read addresses selectively applied to the memory, the write and read addresses being selectively applied based on a write signal output from the memory.

27. (Original) The method of claim 26, wherein the output interlaced scan data is synchronized with the progressive scan data.

28. (Currently Amended) A method of converting progressive scan data to interlaced scan data converter, comprising:

generating count values at a progressive scanning frequency such that the count values are associated with a period of progressive scan data;

generating write addresses for writing progressive scan data into [[the]] a memory based on output of the counter;

generating read addresses for outputting the progressive scan data written into the memory as interlaced scan data;

selectively applying the write and read addresses to the memory based on a write signal generated by the memory;

storing progressive scan data in [[a]] the memory based on the generated write addresses; and

outputting interlaced scan data from the memory based on the generated read addresses.